In the Claims:

1. (Currently Amended) A method for fabricating an integrated pin diode:

producing a doped region of one conduction type which is near a carrier substrate;

producing a doped region remote from the substrate, which is further away from the carrier substrate than the region near the substrate and is of a different conduction type than the conduction type of the region near the substrate;

producing an intermediate region, which is arranged between the region near the substrate and the region remote from the substrate and is undoped or provided with a weak doping in comparison with the doping of the region near the substrate and the doping of the region remote from the substrate;

producing at least one electrically conductive terminal region, which leads to the region near the substrate, in a layer containing the intermediate region;

producing a doped decoupling region at the same time as the region near the substrate, the decoupling region having the same conduction type as the region near the substrate;

producing a circuit arrangement carried by the carrier substrate and containing at least two electronic components; and

producing a circuit substrate, which is arranged between the decoupling region and at least one of the components, and the circuit substrate forming a pn diode or an np diode with the decoupling region,

the decoupling region being arranged between one portion of the components and the carrier substrate and not between the other portion of the components and the carrier substrate, and

in ~~the~~ a layer ~~containing the intermediate region and~~ in which the region near the carrier substrate and the decoupling region are arranged, regions outside the region near the substrate and the decoupling region are provided with a doping of a different conduction type from the region near the substrate and the decoupling region or are undoped.

2. (Previously Presented) The method as claimed in claim 1, wherein the terminal region penetrates through the layer from an interface remote from the substrate as far as an interface near the substrate.

3. (Cancelled)

4. (Currently Amended) The method as claimed in claim 1, comprising ~~the step of~~ producing an electrically conductive decoupling region terminal region at the same time as the production of the terminal region leading to the region near the substrate.

5. (Previously Presented) The method as claimed in claim 4, wherein the decoupling region terminal region and the decoupling region form a shielding well which completely surrounds a region encompassed by the shielding well.

6. (Previously Presented) The method as claimed in claim 4, wherein, in the layer in which the region near the substrate and the decoupling region are arranged, the regions outside the region near the substrate and the decoupling region are provided with a doping of a different conduction type, an oxide covering the region near the substrate and the decoupling region serve for masking implantation.

7. (Currently Amended) The method as claimed in claim 1, wherein at least one of:

the terminal region is produced with fabrication of a trench;

the terminal region is fabricated with the aid of a diffusion process in which dopants diffuse from a region remote from the substrate as far as the layer near the substrate; ~~and~~or

the terminal region is produced by an implantation method.

8. (Currently Amended) The method as claimed in claim 1, wherein at least one of:

the layer containing the intermediate region is produced by an epitaxy method; ~~and~~or

a base material for an embedding region, which serves for embedding components of an integrated circuit arrangement, is produced simultaneously during the epitaxy method.

9. (Currently Amended) The method as claimed in claim 8, wherein an epitaxy method for producing an epitaxial layer is conducted in at least two stages,

the epitaxial growth being interrupted,

the interruption being followed by execution of at least one other process, ~~and~~ or

the growth of the epitaxial layer being continued after the execution of the at least one other process.

10. (Previously Presented) The method as claimed in claim 1, wherein the terminal region leading to the region near the substrate laterally encompasses the intermediate region.

11. (Previously Presented) The method as claimed in claim 1, wherein the layer containing the intermediate region is a semiconductor layer which contains regions with different conduction types.

12. (Previously Presented) The method as claimed in claim 1, wherein the decoupling region adjoins material with a different conduction type or is surrounded by material with a different conduction type.

13. (Currently Amended) An integrated circuit arrangement having a pin diode comprising:

a carrier substrate which carries a region sequence of a pin diode;

a doped region of one conduction type, which is contained in the region sequence and is near the substrate;

a doped region remote from the substrate, which is contained in the region sequence, is further away from the carrier substrate than the region near the substrate, and is of a different conduction type than the conduction type of the region near the substrate;

an intermediate region which is arranged between the region near the substrate and the region remote from the substrate and is undoped or provided with a weak doping in comparison with the doping of the region near the substrate and the doping of the region remote from the substrate;

an electrically conductive terminal region, which leads to the region near the substrate and is arranged in a layer containing the intermediate layer;

a circuit arrangement carried by the carrier substrate and containing at least two electronic components;

a doped decoupling region arranged between one component and the carrier substrate and of the same conduction type as the region near the substrate and arranged in one plane with the region near the substrate; and

a circuit substrate, which is arranged between the decoupling region and at least one of the components, the circuit substrate forming a pn diode or an np diode with the decoupling region,

the decoupling region being arranged between one portion of the components and the carrier substrate and not between the other portion of the components and the carrier substrate, and

in ~~the~~ a layer ~~containing the intermediate layer and~~ in which the region near the substrate and the decoupling region are arranged, regions outside the region near the substrate and the decoupling region are provided with a doping of a different conduction type or are undoped.

14. (Previously Presented) The circuit arrangement as claimed in claim 13, wherein the terminal region penetrates through the layer from an interface remote from the substrate as far as an interface near the substrate.

15. (Previously Presented) The circuit arrangement as claimed in claim 13, wherein the decoupling region has the same dopant concentration as the region near the substrate.

16. (Currently Amended) The circuit arrangement as claimed in claim 15, further comprising an electrically conductive decoupling region terminal region, at least one of:

which leads to the decoupling region; ~~and~~ or

which has the same material composition as the terminal region leading to the region near the substrate.

17. (Cancelled)

18. (Previously Presented) The method as claimed in claim 7, wherein a depth of the trench is at least twice a width of the trench.

19. (Previously Presented) The method as claimed in claim 9, wherein the at least one other process comprises a doping process for fabricating a doping which differs from a doping of the epitaxial layer.

20. (Previously Presented) The method as claimed in claim 10, wherein the terminal region leading to the region near the substrate completely laterally encompasses the intermediate region.

21. (Previously Presented) The method as claimed in claim 12, wherein the decoupling region is surrounded by the material with a different conduction type on all sides apart from one or a plurality of decoupling region terminal regions.

22. (Previously Presented) The method as claimed in claim 4, wherein the decoupling region terminal region and the decoupling region form a shielding well which surrounds a region encompassed by the shielding well, relative to the side areas and the base area of the encompassed region, by at least fifty percent or by at least seventy five percent.